UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,353,438 B2
APPLICATION NO. : 10/645861
DATED : April 1, 2008
INVENTOR(S) : Wingyu Leung et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, FOREIGN PATENT DOCUMENTS, add -- GB 2289779 11/1995 --.

Drawings:

Delete drawing sheet 11 of 11 and substitute therefor the attached Drawing Sheet containing Fig. 11.

Column 1, line 30, amend "Semiconductors" to -- Semiconductor --.

Column 4, line 6, amend "stuck at" to -- stuck-at --.

Column 4, line 28, amend "stuck at" to -- stuck-at --.

Column 9, line 66, replace "**1**" with a comma.

Column 10, lines 27-28, delete "The logic high RESET signal also sets the read pointer value RP provided by toggle flip-flop **313** to a logic."

Column 12, line 66, insert -- **102** -- after "sequencer".

Column 13, line 11, amend "doe" to -- does --.

Column 13, line 38, insert -- to -- before "have".

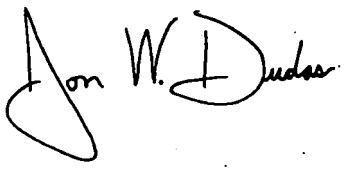
Column 13, line 66, delete "the" (first occurrence).

Column 17, line 33, amend "I11" to -- **111** --.

Column 22, line 54, amend "So" to -- **S0** --.

Signed and Sealed this

Second Day of December, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office

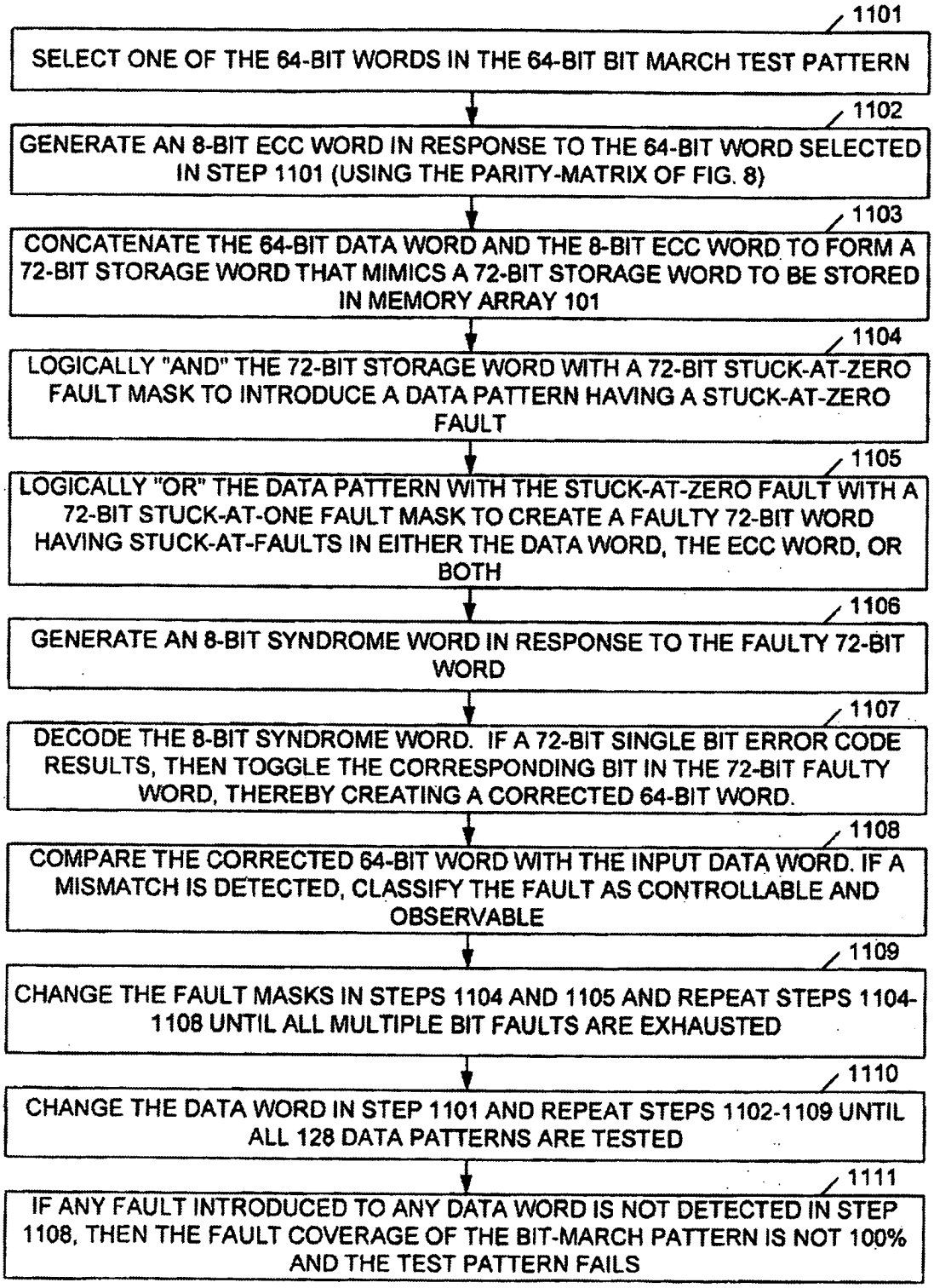

1101
SELECT ONE OF THE 64-BIT WORDS IN THE 64-BIT BIT MARCH TEST PATTERN
1102
GENERATE AN 8-BIT ECC WORD IN RESPONSE TO THE 64-BIT WORD SELECTED IN STEP 1101 (USING THE PARITY-MATRIX OF FIG. 8)
1103
CONCATENATE THE 64-BIT DATA WORD AND THE 8-BIT ECC WORD TO FORM A 72-BIT STORAGE WORD THAT MIMICS A 72-BIT STORAGE WORD TO BE STORED IN MEMORY ARRAY 101
1104
LOGICALLY "AND" THE 72-BIT STORAGE WORD WITH A 72-BIT STUCK-AT-ZERO FAULT MASK TO INTRODUCE A DATA PATTERN HAVING A STUCK-AT-ZERO FAULT
1105
LOGICALLY "OR" THE DATA PATTERN WITH THE STUCK-AT-ZERO FAULT WITH A 72-BIT STUCK-AT-ONE FAULT MASK TO CREATE A FAULTY 72-BIT WORD HAVING STUCK-AT-FAULTS IN EITHER THE DATA WORD, THE ECC WORD, OR BOTH
1106
GENERATE AN 8-BIT SYNDROME WORD IN RESPONSE TO THE FAULTY 72-BIT WORD
1107
DECODE THE 8-BIT SYNDROME WORD. IF A 72-BIT SINGLE BIT ERROR CODE RESULTS, THEN TOGGLE THE CORRESPONDING BIT IN THE 72-BIT FAULTY WORD, THEREBY CREATING A CORRECTED 64-BIT WORD.
1108
COMPARE THE CORRECTED 64-BIT WORD WITH THE INPUT DATA WORD. IF A MISMATCH IS DETECTED, CLASSIFY THE FAULT AS CONTROLLABLE AND OBSERVABLE
1109
CHANGE THE FAULT MASKS IN STEPS 1104 AND 1105 AND REPEAT STEPS 1104-1108 UNTIL ALL MULTIPLE BIT FAULTS ARE EXHAUSTED
1110
CHANGE THE DATA WORD IN STEP 1101 AND REPEAT STEPS 1102-1109 UNTIL ALL 128 DATA PATTERNS ARE TESTED
1111
IF ANY FAULT INTRODUCED TO ANY DATA WORD IS NOT DETECTED IN STEP 1108, THEN THE FAULT COVERAGE OF THE BIT-MARCH PATTERN IS NOT 100% AND THE TEST PATTERN FAILS

FIG. 11